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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 :
H01L 29/00, 29/76, 29/94, 31/062, 31/113, 31/119

A1

(11) International Publication Number: WO 00/68997

(43) International Publication Date: 16 November 2000 (16.11.00)

(21) International Application Number: PCT/US00/12191

(22) International Filing Date: 5 May 2000 (05.05.00)

(30) Priority Data:
60/132,771 6 May 1999 (06.05.99) US

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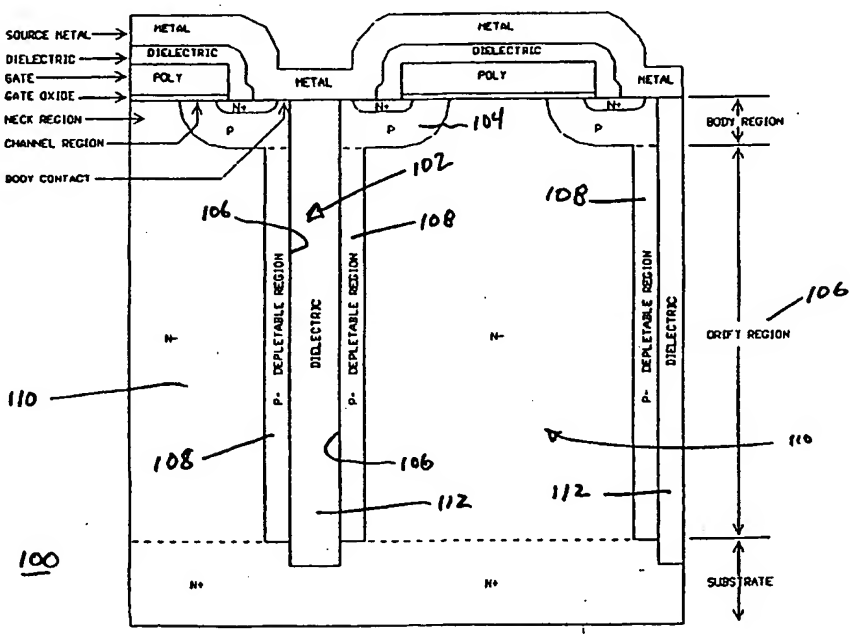
(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: MOSFET WITH FIELD REDUCING TRENCHES IN BODY REGION

(57) Abstract

A MOSFET device (100) that exhibits low power loss characteristics by minimizing source-to-drain channel on resistance includes a semiconductor block having at least two surfaces and a drift region (110) disposed within the semiconductor block; the drift region is characterized by a first conduction type and a first predetermined dopant concentration. A body region (104) with a second conduction type is disposed within the semiconductor block between and adjacent to the first surface and the drift region. A source region (142) is disposed within the semiconductor block, and is embedded in the body region so as to be adjacent to the body region and the first surface. The MOSFET device further includes at least one drain region disposed in the semiconductor block between the second surface and the drift region. An opening is formed in the body region, extending from the first surface and into the semiconductor block. The opening has one or more interior walls (106) that are doped with a dopant of the same conduction type as the body region, and at a second predetermined dopant concentration, so as to form a depletable region near the walls. A blocking voltage applied across the MOSFET device depletes charge carriers within the semiconductor block, so as to substantially prevent electrical current from flowing through the MOSFET between the source region and the drain region. The opening, or trench (102), in the device forces the depletion region to spread laterally within the drift region as blocking voltage increases.



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MOSFET WITH FIELD REDUCING TRENCHES IN BODY REGION

BACKGROUND OF THE INVENTION

The present invention relates to low power loss MOSFET structures, and more particularly, to low power loss MOSFET structures that exhibit low power loss characteristics by minimizing source-to-drain channel on resistance.

FIG. 1 shows a cross section of the structure 10 generally used in prior art high voltage MOSFETs. Current flow through the structure is controlled primarily by the upper portion of the MOSFET structure, including the body 12, source 14, and channel regions 16, and the overlying gate element 18. The power dissipated by a high voltage MOSFET is directly related to the resistance of the path through which the device passes current. Therefore, an important design objective for such a device is minimizing the on-resistance through the structure for a given breakdown voltage. In a high voltage device, the characteristics of the lightly doped region below the body region (hereinafter referred to as the "drift region " 20) determine the breakdown voltage, and are primarily responsible for determining the device on-resistance.

The on-resistance of a device such as that shown in FIG. 1 includes three basic components. They include the resistance of the channel region, the resistance of the neck region, and the resistance of the drift region. A designer can minimize the channel and neck resistances by optimizing the structure geometry, and by shrinking pattern sizes and junction depths to the minimum values that the manufacturing process permits. In low voltage devices, the resistance of the drift region is usually small compared to the channel resistance. As the breakdown voltage increases, however, the contribution of the drift region becomes a larger part of the total. Drift-region resistance increases as $V_b^{2.4}$ to $V_b^{2.6}$ (where V_b is the breakdown voltage), because in order to support the higher breakdown voltage, the drift region must be made both thicker and of higher resistivity material. Breakdown voltage and drift region resistance are inseparably related in this type of structure because they are both controlled by the concentration of dopant atoms, and the thickness, of this region.

The drift region is uniformly doped in the horizontal direction of FIG. 1 across the entire area of the device, and is referred to herein as a uniformly-doped drift

region. In the vertical direction, the dopant concentration is generally uniform, although increasing the dopant concentration toward the bottom of the drift region has been shown to reduce the drift region resistance.

When the voltage applied across the device shown in FIG. 1 is such that the device is in the blocking state (i.e., no carriers flow in the channel region), an electric field (hereinafter referred to as "E-field") exists throughout the device. The breakdown voltage is dependent upon the characteristics of this E-field, and the E-field is dependent upon the dopant concentration and thickness of the drift region; thus, the breakdown voltage is dependant upon the dopant concentration and thickness of the drift region. When the device is in the blocking state, the channel is turned off so there are no carriers entering the drift region from the channel region. Under the influence of the applied voltage, the dopant atoms of the drift region lose their mobile charges and leave behind a depletion region, also referred to as a spacecharge region, consisting of (in the N channel device used as an example in FIG. 1) the fixed negative charges of the P-type dopant atoms of the body region, and the fixed positive charges of the N-type dopant atoms of the drift region. An E-field exists in the spacecharge region which varies in magnitude and reaches its peak at the junction, i.e., at the plane between the positive and negative charges. The E-field at the junction is independent of the distance between the charges, and depends only on the total charge per unit area in each region. In silicon, avalanche breakdown is known to occur when the E-field reaches a value of approximately 20 volts per micron. A charge concentration in the spacecharge region of 1.3×10^{12} electronic charges per square centimeter corresponds to an E-field of approximately 20 volts per micron, regardless of the thickness of the drift region through which these charges are distributed. But the voltage on the device corresponding to an E-field strength of 20 volts per micron is highly dependent upon the thickness of this drift region, because the voltage is equal to the integration of the E-field over the entire thickness of the spacecharge region. To achieve a higher V_b, this same quantity of dopant atoms must therefore be distributed over a thicker layer.

Drift region resistance is controlled by dopant concentration and drift region thickness because the concentration determines how many mobile charges are

available to carry the current, and the thickness determines how far the mobile charges must carry the current. As noted above, the total number of dopant atoms per unit area in the drift region is approximately constant, regardless of the breakdown voltage. For a higher voltage, this same number of dopant atoms, and of mobile charges, is spread over a greater thickness. The specific resistance (resistance multiplied by area) of the drift region is equal to the resistivity multiplied by thickness of the layer. As the same number of dopant atoms is spread through a thicker layer, there is an increase in both resistivity and thickness, so the resistance increases as approximately T^2, while breakdown voltage increases as approximately T, where T represents the thickness of the drift region. As described hereinbefore, the drift-region resistance increases as $V_b^{2.4}$ to $V_b^{2.6}$ This relationship between drift-region resistance and breakdown voltage is due to the fact that carrier mobility increases as dopant concentration decreases, causing avalanche breakdown to occur at lower E-field magnitudes in higher voltage devices.

FIG. 2 shows a plot 22 of the lower limit of specific resistance for this structure with a fully-optimized dopant profile in the drift region. Even if the channel resistance and the neck resistance are reduced to zero, the on-resistance of a silicon device made with the structure of FIG. 1 can not be made lower than this value.

FIG. 3 shows a vertical channel version of a prior art high voltage MOSFET 24, also known as a Trench-MOS or U-MOS. This structure reduces both the channel resistance and the neck resistance, producing significant reductions of on-resistance in low-voltage devices, but it is of little or no benefit to high voltage devices because it still has the same drift resistance as the structure shown in FIG. 1, and so is governed by the same relationship between specific resistance and breakdown voltage.

FIG. 4 shows a prior art structure that can overcome the limits described for the structure shown in FIG. 2. This is a conductivity-modulated field effect transistor 26, more commonly known as an insulated gate bipolar transistor (hereinafter referred to as "IGBT"). The drift region 20 of this structure is subject to the same dopant concentration limits as the MOSFET structure 10 of FIG. 1, but it achieves a higher concentration of carriers during conduction by injecting both positive and negative mobile charges during conduction. The mobile negative charges come in through the

channel, just as they do in an ordinary MOSFET, but the mobile positive charges come in from the P emitter region 28 at the bottom of the structure. During conduction, the concentration of these mobile positive charges can be more than an order of magnitude greater than the concentration of the fixed positive charges, so the conductivity can be correspondingly higher, and the specific resistance correspondingly lower. When the channel is turned off the mobile negative charges stop coming in, and without these, the barrier rebuilds on the P emitter junction, causing the mobile positive charges to also stop coming in. When all these excess charges have been depleted, the device is left with the voltage supported on the same fixed positive charge distribution as in the MOSFET. Although this device has a very significantly lower specific resistance than the MOSFET, it has a major disadvantage in high frequency applications because of the time required to remove all the excess charges each time the device makes the transition from the conducting state to the blocking state.

FIG. 5 shows another prior art structure 30 which can overcome the limits of the structure 10 of FIG. 1. The structure of FIG. 5 is an example of an Alternating Conductivity Vertical Layer (hereinafter referred to as "ACVL") drift region. This structure is described in U.S. Patent No. 5,438,215, entitled "POWER MOSFET" and invented by J. Tihanyi, and also in "*A New Generation of High Voltage MOSFETS Breaks the Limit Line of Silicon*", by G. Deboy, M. Marz, J Stengl, H. Strack, J. Tihani, and H. Weber, presented December 9, 1998 at the International Electron Devices Meeting in San Francisco. A U-MOS version of this structure is described in "*Simulated Superior Performances of Semiconductor Superjunction Devices*," by Tatsuhiko Fujihira and Yashushi Miyasaka, presented at the 1998 International Symposium on Power Semiconductor Devices in Kyoto, Japan. This structure, like that of the structure shown in FIG. 4, increases the drift region conductivity by increasing the concentration of mobile negative charges. In both cases, these additional negative charges must be balanced by additional positive charges. In the FIG. 4 structure, they are balanced by mobile positive charges, while in the FIG. 5 structure they are balanced by fixed positive charges.

The structure shown in FIG. 5 decreases the drift region resistance by placing additional N-type dopant atoms in the drift region 20 (fixed positive charges) and counterbalancing them with P-type dopant atoms (fixed negative charges) in such a way that the fixed charges neutralize each other when the device is blocking, and the N-type mobile charges participate in the current flow when the device is conducting. This neutralization is accomplished by locating the N and P type dopant atoms in alternating vertical layers 32, so that the high-voltage junction is folded up and down vertically many times across the area of the device. When the device transitions to the blocking state, the spacecharge region spreads horizontally outward from these vertical junctions. The dopant concentration in each vertical layer is kept low enough so that the layer is fully depleted before the resulting horizontal E-field is high enough to cause a horizontal avalanche breakdown. After the drift region is fully depleted by this horizontal movement, the vertical E-field continues to build up by ionizing the dopant atoms above and below the vertical layers 32. Breakdown then occurs only after the vertical E-field reaches the field strength needed for avalanche (hereinafter referred to as "critical field strength"). During conduction, the fixed charges in both the N and P vertical layers 32 are neutralized by mobile charge carriers, but only the carriers in the N type layers participate in current flow. The vertical resistance of each N layer is approximately the same, no matter what its horizontal thickness, so the lower limit for on-resistance is determined only by how thin these vertical alternating layers can be made, because this determines how many vertically-conducting layers can be placed within the horizontal area of the device.

FIG. 5 also shows the horizontal and vertical E-fields in the uniformly-doped device and the ACVL device. In the uniformly-doped device, the horizontal E-field is everywhere zero, while in the ACVL device the horizontal E-field reaches its peak values at the vertical junctions, with these peaks ideally being just below the critical field strength. In each case, the peak vertical E-field is the critical field strength, above which avalanche breakdown occurs. In the ACVL structure, the E-field remains close to this value over the entire drift region, while in the uniformly-doped structure it decreases linearly with increasing distance from the junction. Since the integration of the E-field over the entire region (i.e., the area beneath the E field

curve) represents the total voltage that the structure supports, the ACVL structure can support a higher voltage on the same drift region thickness, or equivalently, it can support the same voltage on a thinner drift region.

Although the structure shown in FIG. 5 can theoretically produce a very low specific resistance, practical shortcomings exist that limit the usefulness of the structure. The structure is inherently difficult to build, i.e., to distribute the necessary dopant atoms into these vertical layers. Another even more significant fabrication problem is that the number of dopant atoms per unit area in the vertical P layers must precisely match the number in the N layers, so that both layers deplete simultaneously. If one layer becomes fully depleted before its neighboring opposite-conductivity layer, the mobile charges in the undepleted vertical layer will allow current to flow vertically, causing an increased field at its top or bottom end, and a reduction in breakdown voltage.

Other similar structures that exhibit low specific resistance are described in U.S. patents No.5,539,238, No.5,569,949, No.5,640,034, No.5,696,010, and No.5,723,891.

It is an object of the present invention to substantially overcome the above-identified disadvantages and drawbacks of the prior art.

SUMMARY OF THE INVENTION

The foregoing and other objects are achieved by the invention which in one aspect comprises a MOSFET device that includes a semiconductor block having at least a first surface and a second surface, and a drift region disposed within the semiconductor block, having a first conduction type and a first predetermined dopant concentration. At least one body region with a second conduction type is disposed within the semiconductor block between and adjacent to the first surface and the drift region. At least one source region is disposed within the semiconductor block, and is embedded in the body region so as to be adjacent to the body region and the first surface. The MOSFET device further includes at least one drain region disposed in the semiconductor block between the second surface and the drift region. At least one opening is formed in the body region, extending from the first surface and into the

semiconductor block. The opening has one or more interior walls that are doped with a dopant of the same conduction type as the body region, and at a second predetermined dopant concentration, so as to form a depletable region near the walls. A blocking voltage applied across the MOSFET device depletes charge carriers within the semiconductor block, so as to substantially prevent electrical current from flowing through the MOSFET between the source region and the drain region.

In another embodiment of the invention, a total quantity of a dopant in the depletable region, when integrated horizontally from an edge adjacent to the drift region to an edge formed by the interior wall of the at least one opening, is substantially equal to a total quantity of a dopant in the drift region, when integrated horizontally from an edge adjacent to one of the doped walls to a center of the drift region.

In another embodiment of the invention, a total quantity of a dopant in the depletable region, when integrated horizontally from an edge adjacent to the drift region to an edge formed by the interior wall of the at least one opening, is less than a total quantity of a dopant in the drift region, when integrated horizontally from an edge adjacent to one of the doped walls to a center of the drift region.

In another embodiment of the invention, the opening is filled with a dielectric material.

In another embodiment of the invention, the dielectric includes borosilicate glass, such that a required amount of boron from the borosilicate glass provides the dopant for the walls.

In another embodiment of the invention, the opening extends into the semiconductor block at least to the drain region.

In another embodiment of the invention, the depletable region contacts the body region, such that the body region and the depletable region form a substantially continuous region of the second conduction type.

Another embodiment of the invention further includes at least one voltage divider disposed within the opening. The voltage divider has a first end adjacent to the first surface and electrically coupled to a source metal, a second end extending

through the opening and into the drain region, and at least one exterior side surface in contact with the one or more interior walls of the opening.

In another embodiment of the invention, the voltage divider distributes a voltage applied across the MOSFET device uniformly over the interior wall from the first surface to the drain region.

In another embodiment of the invention, the voltage divider distributes a voltage applied across the MOSFET device non-uniformly over the drift region from the first surface to the drain region.

In another embodiment of the invention, the voltage divider concentrates the voltage at the second end, proximate to the drain region.

In another embodiment of the invention, the voltage divider is selected from the group consisting of capacitive voltage dividers, resistive voltage dividers, stacked semiconductor junction voltage dividers, and combinations thereof.

In another embodiment of the invention, the voltage divider includes a resistive voltage divider characterized by one or more linear resistors.

In another embodiment of the invention, the voltage divider includes a resistive voltage divider characterized by one or more non-linear resistors.

In another embodiment of the invention, the voltage divider includes a resistive voltage divider characterized by a combination of one or more linear resistors and one or more non-linear resistors.

In another embodiment of the invention, the source region is embedded in the body region so as to exclude a center region of the source region. A portion of the body region extends through the source region and contacts the first surface.

In another embodiment of the invention, the opening is formed within the portion of the body region that extends through the source region.

In another embodiment of the invention, the source region is embedded in the body region such that within the source region, substantially none of the body region contacts the first surface.

In another embodiment of the invention, the opening extends from the first surface through the source region, into the body region and through the drift region.

In another embodiment of the invention, a source metal contact extends into the opening, so as to form an electrical contact with the body region.

In another aspect, the invention comprises a MOSFET device, including a semiconductor block having at least a first surface and a second surface, and a drift region disposed within the semiconductor block and having a first conduction type and a first predetermined dopant concentration. At least one body region, having a second conduction type, is disposed within the semiconductor block between and adjacent to the first surface and the drift region. At least one source region is disposed within the semiconductor block. The source region is embedded in the at least one body region so as to be adjacent to the body region and the first surface. At least one drain region is disposed in the semiconductor block between the second surface and the drift region. The MOSFET device further includes at least one opening in the body region, extending from the first surface into the semiconductor block and having one or more interior walls. At least one voltage divider is disposed within the opening. The voltage divider has a first end adjacent to the first surface and electrically coupled to a source metal, a second end extending through the opening and into the drain region, and at least one exterior side surface in contact with the one or more interior walls of the opening. A blocking voltage applied across the MOSFET device depletes charge carriers within the semiconductor block, so as to substantially prevent electrical current from flowing through the MOSFET between the source region and the drain region.

In another embodiment of the invention, a total quantity of a dopant in the depletable region, when integrated horizontally from an edge adjacent to the drift region to an edge formed by the interior wall of the at least one opening, is substantially equal to a total quantity of a dopant in the drift region, when integrated horizontally from an edge adjacent to one of the doped walls to a center of the drift region.

In another embodiment of the invention, a total quantity of a dopant in the depletable region, when integrated horizontally from an edge adjacent to the drift region to an edge formed by the interior wall of the at least one opening, is less than a

total quantity of a dopant in the drift region, when integrated horizontally from an edge adjacent to one of the doped walls to a center of the drift region.

BRIEF DESCRIPTION OF DRAWINGS

The foregoing and other objects of this invention, the various features thereof, as well as the invention itself, may be more fully understood from the following description, when read together with the accompanying drawings in which:

FIG. 1 shows a cross section of the structure generally used in prior art high voltage MOSFETs;

FIG. 2 shows a plot of the lower limit of specific resistance for the structure shown in FIG. 1 with a fully-optimized dopant profile in the drift region;

FIG. 3 shows a vertical channel version of the prior art high voltage MOSFET of FIG. 1;

FIG. 4 shows a prior art structure that can overcome the limits described for the structure shown in FIG. 2;

FIG. 5 shows another prior art structure which can overcome the limits of the structure of FIG. 2;

FIG 6 shows a sectional view of one preferred embodiment of a high voltage MOSFET structure according to this invention;

FIG 7 shows a sectional view of another preferred embodiment of the structure shown in FIG. 6, further including a voltage divider within the trench;

FIG. 8 shows a sectional view of another preferred embodiment of the structure shown in FIG. 6, further including a voltage divider and excluding the dopant within the trench walls; and,

FIG. 9 shows a sectional view of another preferred embodiment of the structure shown in FIG. 6, where the source region completely covers the body region.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG 6 shows a sectional view of one preferred embodiment of a high voltage MOSFET structure 100 according to this invention. In one preferred embodiment, FIG. 6 represents a cross section through a circular top surface geometry, although in

other embodiments, the same cross section could be used to represent any of a variety of alternate top-surface geometries, such as stripes, rectangles, squares, hexagons, or other polygonal or irregular patterns.

The structure shown in FIG. 6 includes a trench 102 or other suitable opening having a depth greater than its width. The opening is referred to herein in general as a trench, regardless of its shape. The trench 102 may be etched into the center of the body region 104, or alternately the trench 102 may be formed in other parts of the body region 104 by other methods known to those in the art. The walls 106 of this opening are doped with the same type of dopant used in the body (P-type, in the case of the exemplary P-channel MOSFET in FIG. 1) but at a concentration low enough so the depletion region spreads horizontally completely through this layer before the device transitions into an avalanche breakdown state. The horizontally integrated dopant quantity in these P-type layers 108 (also referred to herein as depletable regions) should be equal to, or less than, the horizontally integrated dopant quantity in each half of the adjacent N-layer 110 (also referred to herein as the drift region). The optimum relationship between the breakdown voltage and the specific resistance occurs when the dopant quantities in these adjacent layers are exactly equal, but a very significant improvement can be achieved even if they are not equal, provided the quantity of body-region dopant is less than that of the drain-region dopant.

Significant improvements in specific resistance versus breakdown voltage can he achieved by forcing the depletion region to spread laterally, rather than vertically, over the drift region. This new structure is similar to the previously described ones with regard to utilizing a laterally spreading depletion region, but is different as to the location of the trench structure which produces this spread. In the copending application, the trench 102 is located in the area where the drain region meets the top surface of the device. In the new structures of the present invention, the trench is located in the area where the body region, rather than the drain region, meets the top surface of the device. One advantage of this configuration is that it is more readily incorporated into the high-voltage MOSFET structures being manufactured today. Another advantage is more efficient area utilization.

In most recent prior art structures, the region where the drain meets the top surface is covered by the gate polysilicon, and the channel regions feed current into this drain region from both sides. This region where the drain meets the top surface is often referred to as the "neck region". In the structures described in the copending application, the polysilicon over the neck region must be split into two portions, so the trench can be located between them. Also, a separate electrical contact must be added to establish the necessary connection of the source metal to the trench structure. In the structures which are the subject of the present invention, there is no need for a new opening in the polysilicon because the trench 102 is located in the already-existing opening over the body region 104, and there is no need for a new contact region because the source metal connects to the trench structure 102 in the existing body contact opening. This new structure could even be added to existing device structures without changing the photomasks or process, other than by adding a photomask to etch the trenches, and adding the processes required to fill them.

FIG. 6 shows a structure in which the trench walls 106 have been doped, after etching, with the required low dose of P-type dopant, and then the trench has been filled with dielectric 112. In some embodiments, the structure may use borosilicate glass as the dielectric 112 to fill the trenches. The semiconductor wafers may then be heated to the point where the required amount of boron diffuses from the glass into the silicon to form the P-type regions 108.

FIG. 7 shows a similar structure 120, but with a voltage divider 122 also included in the trench, to make the achievement of optimum performance less sensitive to the quantity of P-type dopant. The voltage divider 122 might consist of material such as a layer of SIPOS (semi-insulating polysilicon) deposited directly on the trench sidewalls, or a resistive film such as vanadium oxide deposited over a dielectric film on the sidewalls 106. The voltage divider 122 might also be made by using borosilicate glass as both dielectric and diffusion source.

FIG. 8 shows a structure 130similar to the structure 120 shown in FIG. 7, but with the voltage divider 122 only, without the P-type regions 108 on the trench sidewalls 106 that are present in the structure 120 of FIG. 7.

FIG. 9 shows a structure 140 which is the same as FIG. 1 except that, in order to save a photomask, the N^+ source 142 has been deposited entirely across the polysilicon opening, rather than being excluded from the center and exposing the body region 104 in FIGs. 6, 7 and 8. When the trench 102 is etched, it goes through the N^+ and exposes the body region 104 on the trench sidewalls 106. The required contact to the body region 104 is then made by etching the dielectric 112 from the top of the trench 102, enabling the source metal 144 to contact the body region 104 beneath the N^+ source 142. Such a process could also be used with the structures of FIGs. 7 and 8 to create alternate embodiments. In such embodiments, the upper portion of the voltage divider 122 would be etched or otherwise removed from the trench 102, so as to allow source metal 144 to extend into the trench 102 and create an electrical contact with the body region 104 and the voltage divider122

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of the equivalency of the claims are therefore intended to be embraced therein.

What is claimed is:

1. A MOSFET device, comprising:

a semiconductor block having at least a first surface and a second surface;

a drift region disposed within said semiconductor block, having a first conduction type and a first predetermined dopant concentration;

at least one body region, having a second conduction type, disposed within said semiconductor block between and adjacent to said first surface and said drift region;

at least one source region disposed within said semiconductor block, embedded in said at least one body region so as to be adjacent to said body region and said first surface;

at least one drain region disposed in said semiconductor block between said second surface and said drift region; and,

at least one opening in said body region, extending from said first surface into said semiconductor block and having one or more interior walls, said walls being doped with a dopant of the same conduction type as said body region and at a second predetermined dopant concentration, so as to form a depletable region near said walls; wherein a blocking voltage applied across said MOSFET device depletes charge carriers within said semiconductor block, so as to substantially prevent electrical current from flowing through said MOSFET between said source region and said drain region.

2. A MOSFET device according to claim 1, wherein a total quantity of a dopant in said depletable region, when integrated horizontally from an edge adjacent to said drift region to an edge formed by said interior wall of said at least one opening, is substantially equal to a total quantity of a dopant in said drift region, when integrated horizontally from an edge adjacent to one of said doped walls to a center of said drift region.

3. A MOSFET device according to claim 1, wherein a total quantity of a dopant in said depletable region, when integrated horizontally from an edge adjacent to said drift region to an edge formed by said interior wall of said at least one opening, is less than a total quantity of a dopant in said drift region, when integrated horizontally from an edge adjacent to one of said doped walls to a center of said drift region.

4. A MOSFET device according to claim 1, wherein said opening is filled with a dielectric material.

5. A MOSFET device according to claim 4, wherein said dielectric includes borosilicate glass, such that a required amount of boron from said borosilicate glass provides said dopant for said walls.

6. A MOSFET device according to claim 1, wherein said opening extends into said semiconductor block at least to said drain region.

7. A MOSFET device according to claim 1, wherein said depletable region contacts said body region, such that said body region and said depletable region form a substantially continuous region of said second conduction type.

8. A MOSFET device according to claim 1, further including at least one voltage divider disposed within said opening, said voltage divider having a first end adjacent to said first surface and electrically coupled to a source metal, a second end extending through said opening and into said drain region, and at least one exterior side surface in contact with said one or more interior walls of the opening.

9. A MOSFET device according to claim 8, wherein said voltage divider distributes a voltage applied across said MOSFET device uniformly over said interior wall from said first surface to said drain region.

10. A MOSFET device according to claim 8, wherein said voltage divider distributes a voltage applied across said MOSFET device non-uniformly over said drift region from said first surface to said drain region.

11. A MOSFET device according to claim 10, wherein said voltage divider concentrates said voltage at said second end, proximate to said drain region.

12. A MOSFET device according to claim 8, wherein said voltage divider is selected from the group consisting of capacitive voltage dividers, resistive voltage dividers, stacked semiconductor junction voltage dividers, and combinations thereof.

13. A MOSFET device according to claim 8, wherein said voltage divider includes a resistive voltage divider characterized by one or more linear resistors.

14. A MOSFET device according to claim 8, wherein said voltage divider includes a resistive voltage divider characterized by one or more non-linear resistors.

15. A MOSFET device according to claim 8, wherein said voltage divider includes a resistive voltage divider characterized by a combination of one or more linear resistors and one or more non-linear resistors.

16. A MOSFET device according to claim 1, said source region being embedded in said body region so as to exclude a center region of said source region, wherein a portion of said body region extends through said source region and contacts said first surface.

17. A MOSFET device according to claim 16, wherein said opening extends through said portion of said body region that extends through said source region.

18. A MOSFET device according to claim 1, said source region being embedded in said body region such that within said source region, substantially none of said body region contacts said first surface.

19. A MOSFET device according to claim 18, wherein said opening extends from said first surface through said source region, into said body region and through said drift region.

20. A MOSFET device according to claim 19, wherein a source metal contact extends into said opening, so as to form an electrical contact with said body region.

21. A MOSFET device, comprising:

a semiconductor block having at least a first surface and a second surface;

a drift region disposed within said semiconductor block, having a first conduction type and a first predetermined dopant concentration;

at least one body region, having a second conduction type, disposed within said semiconductor block between and adjacent to said first surface and said drift region;

at least one source region disposed within said semiconductor block, embedded in said at least one body region so as to be adjacent to said body region and said first surface;

at least one drain region disposed in said semiconductor block between said second surface and said drift region; and,

at least one opening in said body region, extending from said first surface into said semiconductor block and having one or more interior walls, and at least one voltage divider disposed within said opening, said voltage divider having a first end adjacent to said first surface and electrically coupled to a source metal, a second end extending through said opening and into said drain region, and at least one exterior

side surface in contact with said one or more interior walls of the opening;

wherein a blocking voltage applied across said MOSFET device depletes charge carriers within said semiconductor block, so as to substantially prevent electrical current from flowing through said MOSFET between said source region and said drain region.

22. A MOSFET device according to claim 21, wherein a total quantity of a dopant in said depletable region, when integrated horizontally from an edge adjacent to said drift region to an edge formed by said interior wall of said at least one opening, is substantially equal to a total quantity of a dopant in said drift region, when integrated horizontally from an edge adjacent to one of said doped walls to a center of said drift region.

23. A MOSFET device according to claim 21, wherein a total quantity of a dopant in said depletable region, when integrated horizontally from an edge adjacent to said drift region to an edge formed by said interior wall of said at least one opening, is less than a total quantity of a dopant in said drift region, when integrated horizontally from an edge adjacent to one of said doped walls to a center of said drift region.

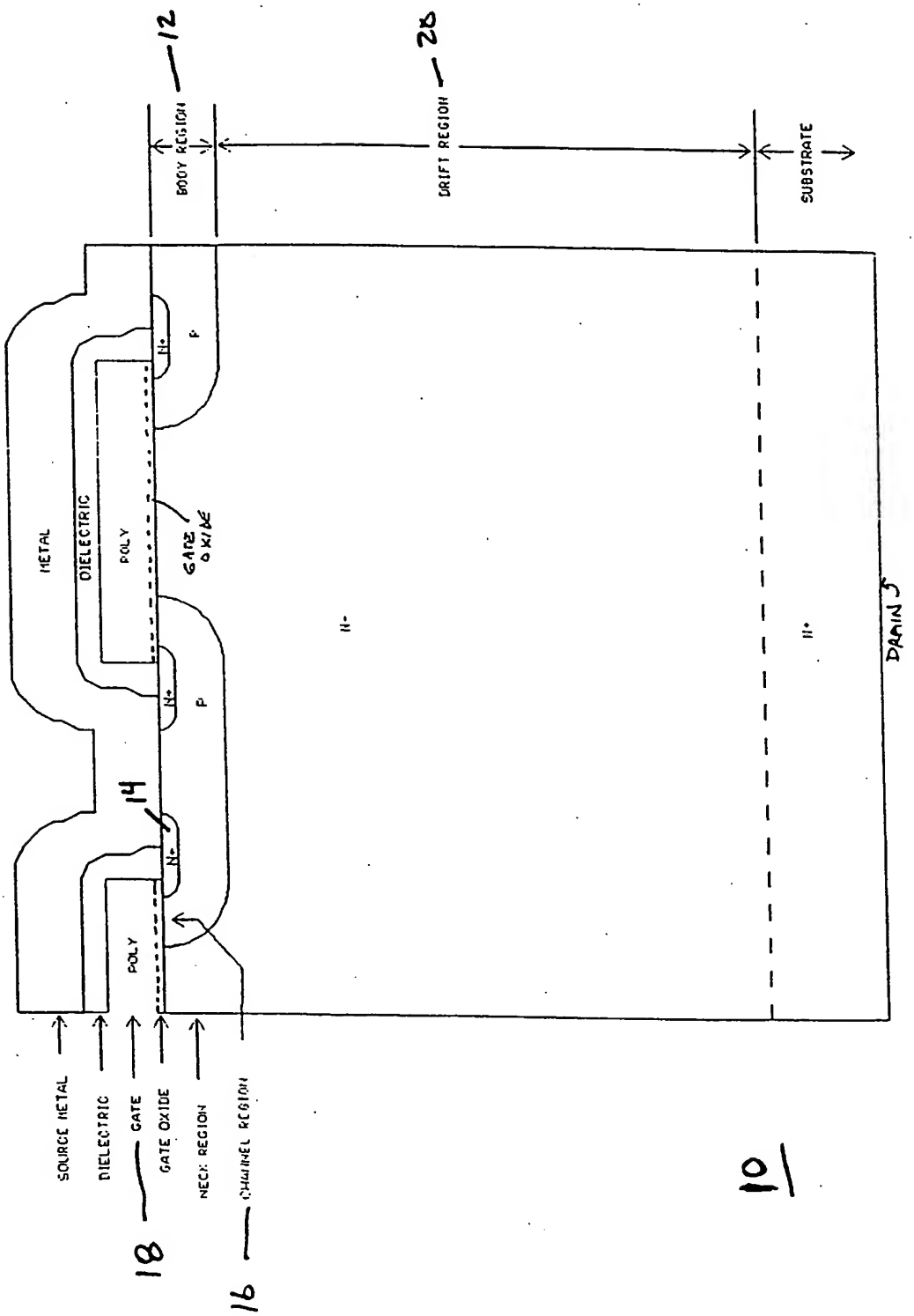


FIG. 1
(PRIOR ART)

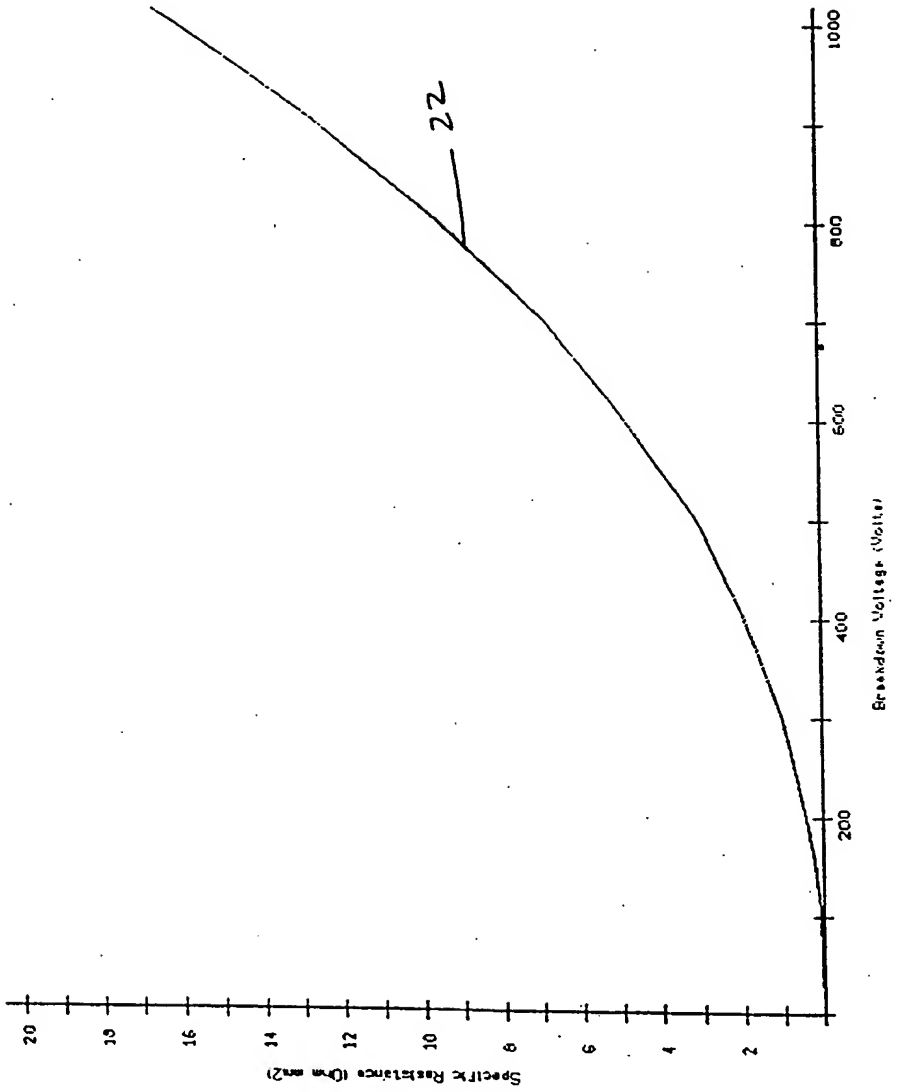


FIG. 2
(PRIOR ART)

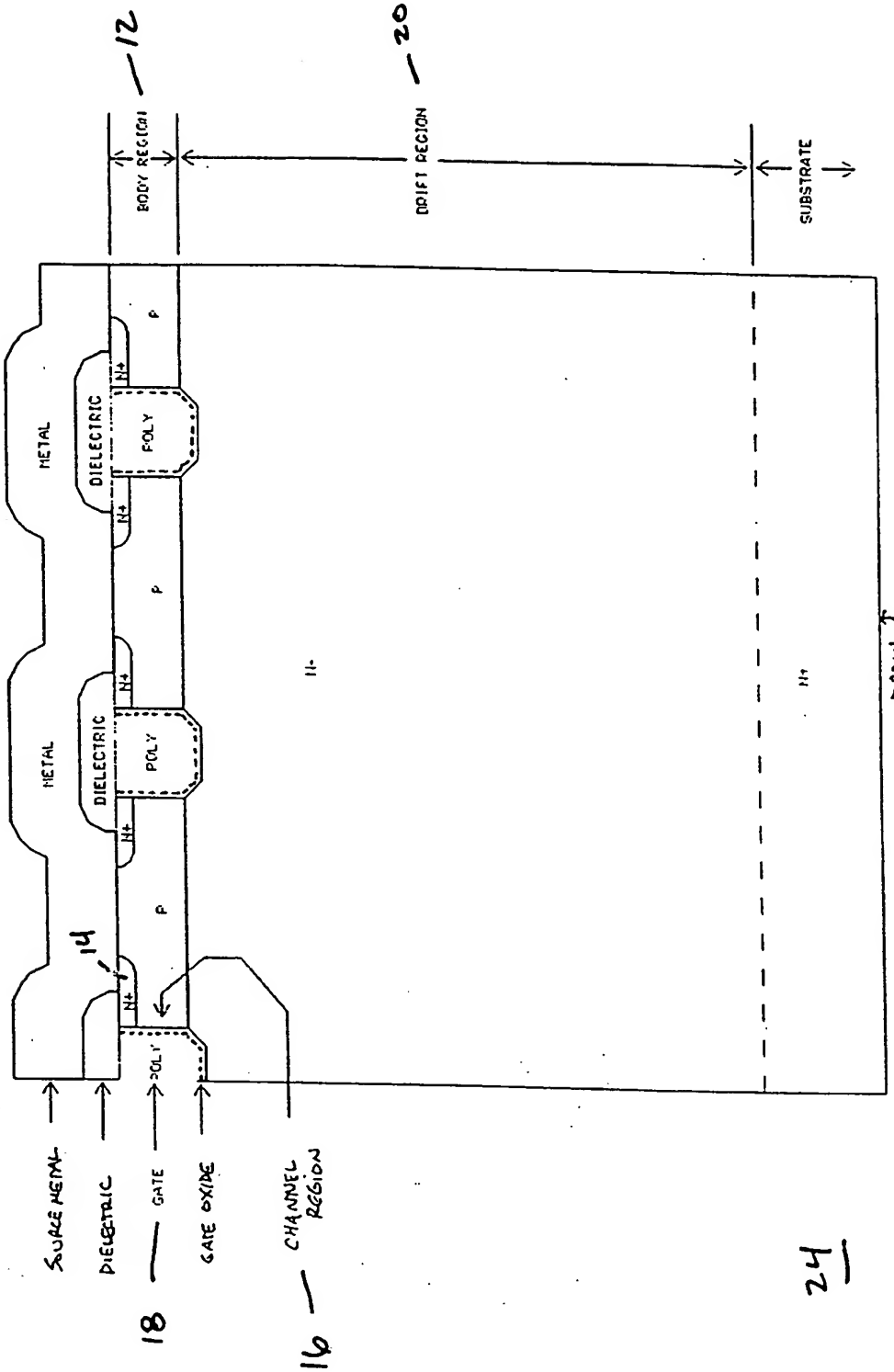


FIG. 3
(PRIOR ART)

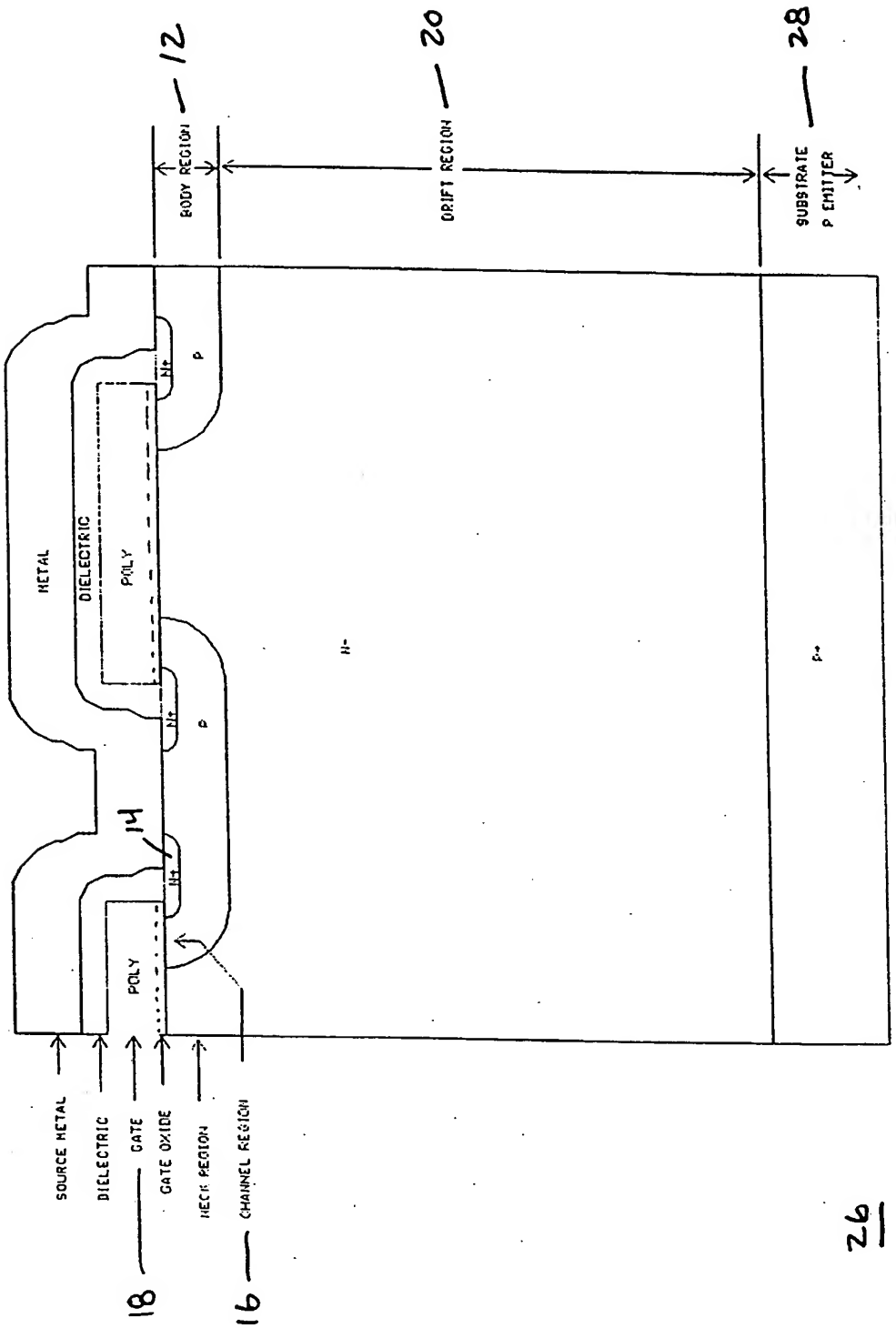


FIG. 4
(PRIOR ART)

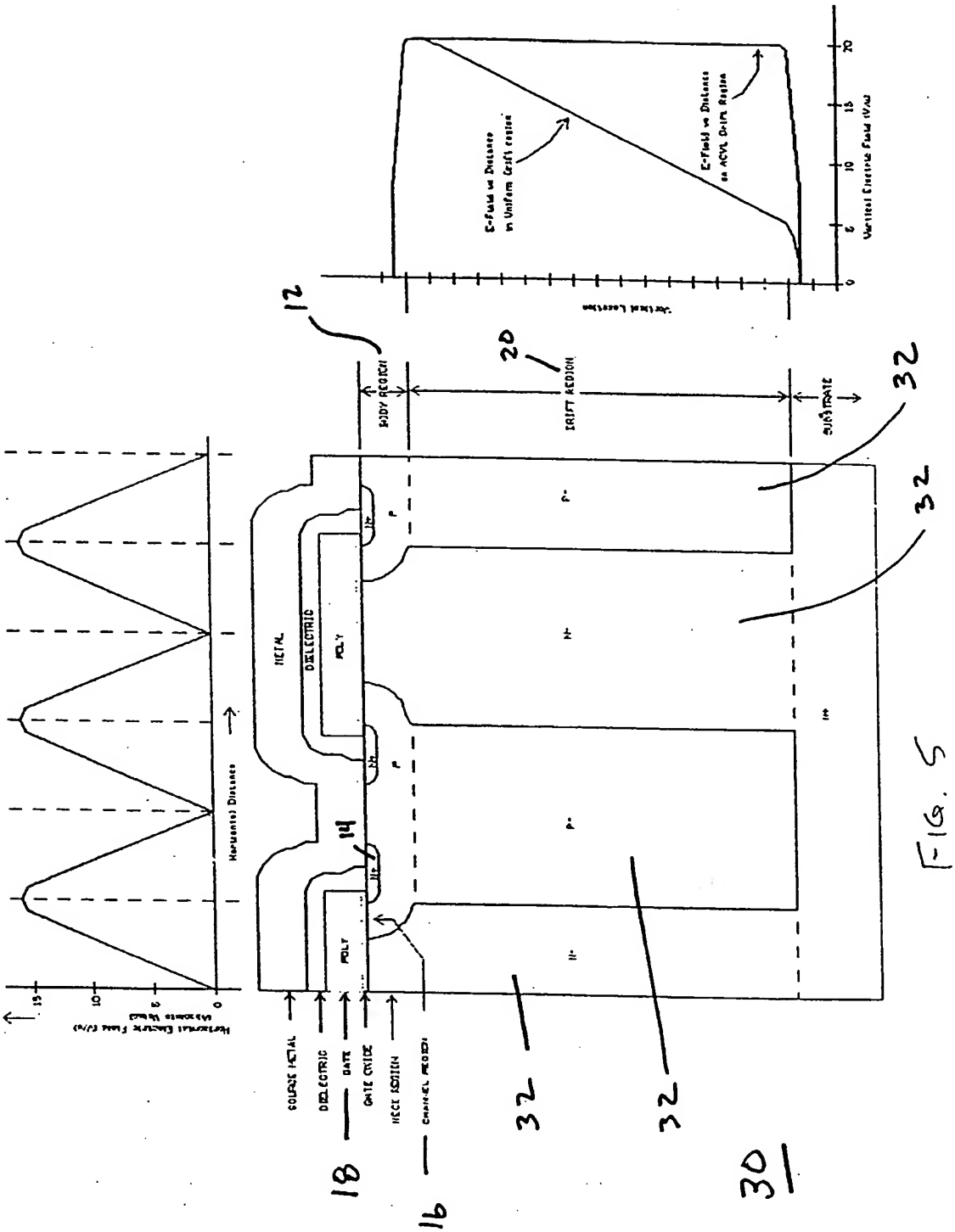
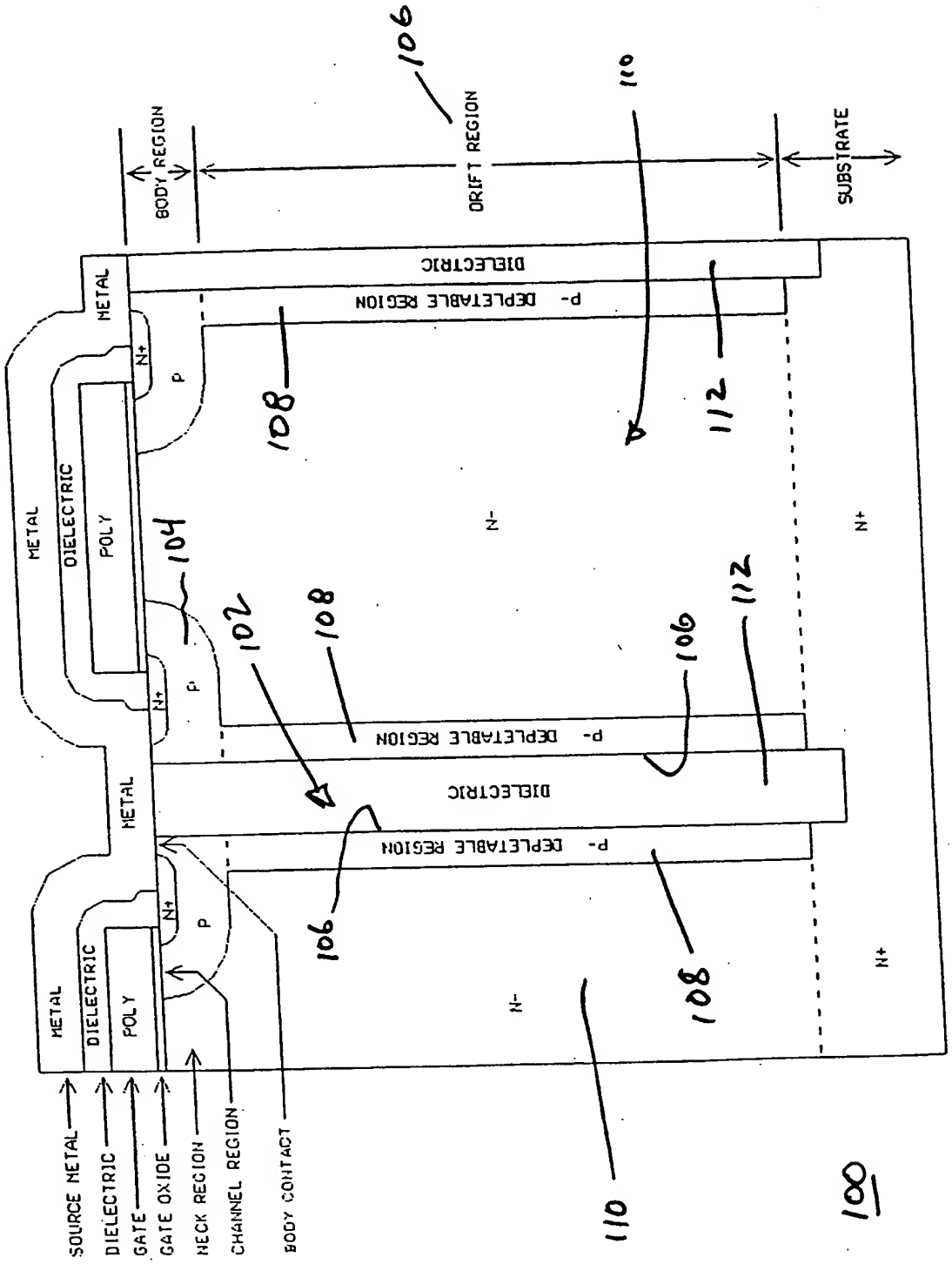


FIG. 5
(PRIOR ART)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DRIFT REGION
110
BODY REGION
SUBSTRATE
DIELECTRIC
P- DEPLETABLE REGION
METAL
N+
P
108
112
DIELECTRIC
POLY
104
N-
N+
102
106
SOURCE METAL
DIELECTRIC
GATE
GATE OXIDE
NECK REGION
CHANNEL REGION
BODY CONTACT
100

FIG. 6

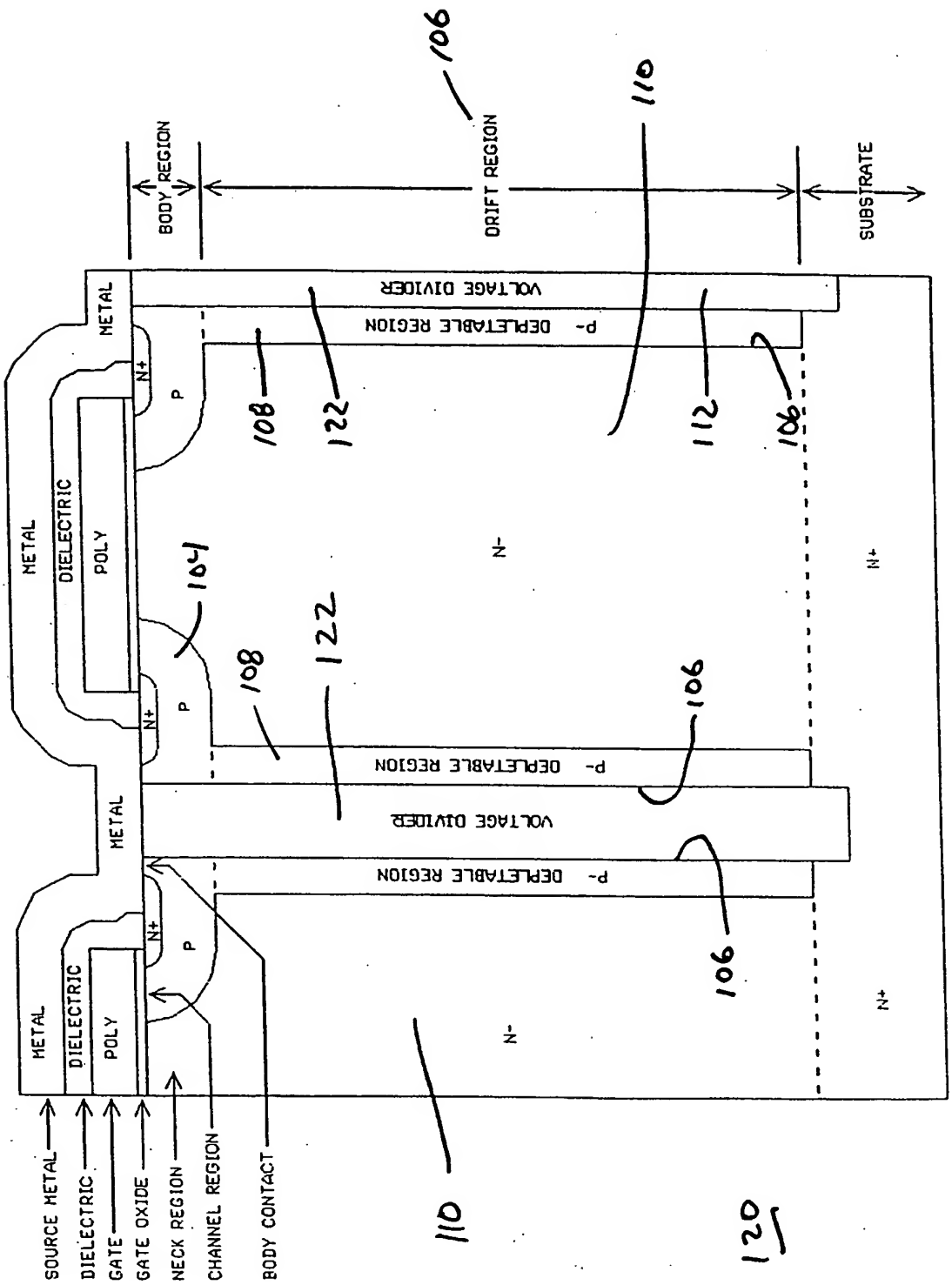
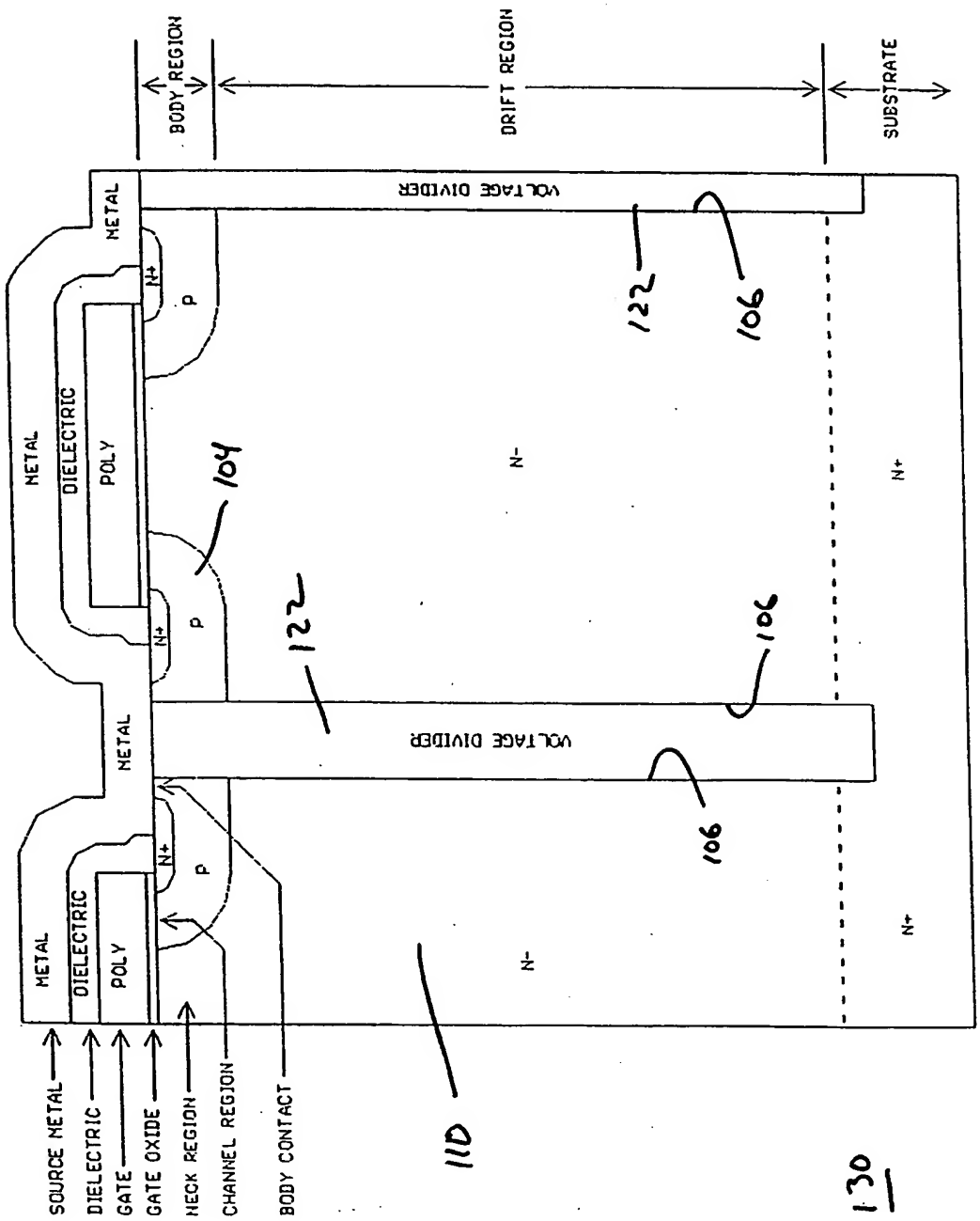

106
110
BODY REGION
DRIFT REGION
SUBSTRATE
METAL
DIELECTRIC
POLY
N+
P
VOLTAGE DIVIDER
P- DEPLETABLE REGION
108
122
112
106
104
N-
N+
110
120
SOURCE METAL
DIELECTRIC
GATE
GATE OXIDE
NECK REGION
CHANNEL REGION
BODY CONTACT

FIG. 7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DRIFT REGION
SUBSTRATE
METAL
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POLY
N+
P
N-
VOLTAGE DIVIDER
122
106
104
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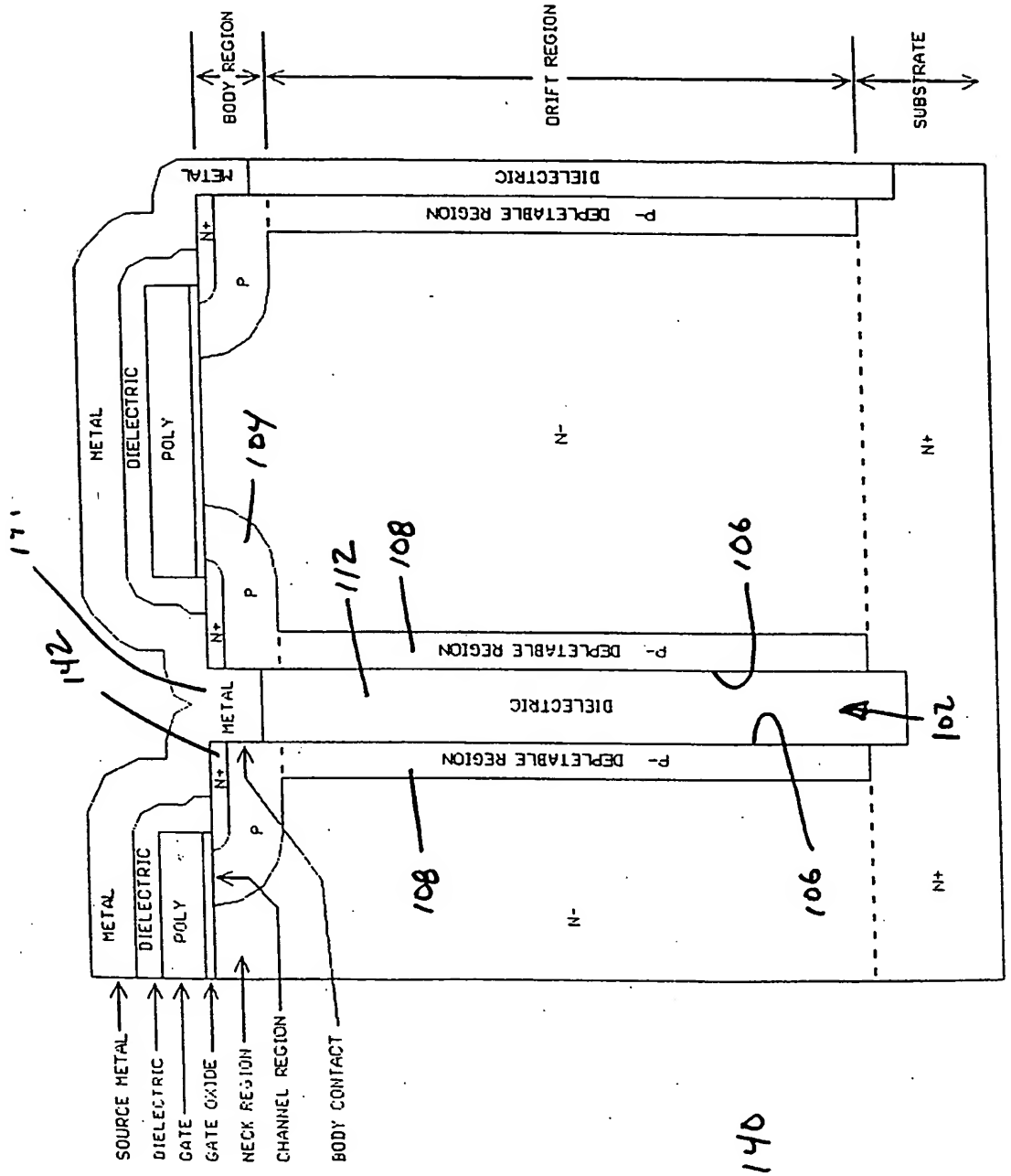
SOURCE METAL
DIELECTRIC
GATE
GATE OXIDE
NECK REGION
CHANNEL REGION
BODY CONTACT

FIG. 8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SUBSTRATE
METAL
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DEPLETABLE REGION
P-
N+
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N-
POLY
104
112
108
106
102
142
140
SOURCE METAL
DIELECTRIC
GATE
GATE OXIDE
NECK REGION
CHANNEL REGION
BODY CONTACT

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/12191

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 29/00, 29/76, 29/94; 31/062, 31/113, 31/119
US CL : 257/327, 328, 329, 333, 504, 505, 508, 536
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/327, 328, 329, 333, 504, 505, 508, 536

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO APS EAST, search terms: trench; vertical; BPSG

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,623,152 A (MAJUMDAR et al.) 22 April 1997 (22.04.1997), Figs. 1, 5-9, 11 and col. 5-10.	1-15, 18-23
Y	US 5,569,949 A (MALHI) 29 October 1996 (29.10.1996), Figs. 2, 4, 6, 7 and col. 2-5.	1-15, 18-23
Y	US 5,306,940 A (YAMAZAKI) 26 April 1994 (26.04.1994), Fig. 4B; col. 4, lines 28-48.	5
A	US 5,789,769 A (YAMAZAKI) 04 August 1998 (04.08.1998), Fig. 7.	1-23
A	US 5,519,241 A (OPPERMANN et al.) 21 May 1996 (21.05.1996), Fig. 1.	1-23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search
08 JULY 2000

Date of mailing of the international search report
30 AUG 2000

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